IN THE CLAIMS

Please amend claim 41 as follows below.

Please add new claims 43-58 as follows below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1-36. (Cancelled)

37. (Previously Presented) A pipelined instruction decoder for a multithread processor, the pipelined instruction decoder comprising:

an instruction decode pipeline to decode instructions associated with a plurality of instruction threads, the instruction decode pipeline having a predetermined number of pipe stages;

a valid bit pipeline in parallel with the instruction decode pipeline, the valid bit pipeline having the same predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline, the valid bit pipeline to associate a valid indicator at each pipe stage with each instruction being decoded in the instruction decode pipeline; and

a thread identification pipeline in parallel with the instruction decode pipeline and the valid bit

pipeline, the thread identification pipeline having the same predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline and the valid bit pipeline, the thread identification pipeline to associate a thread identification at each pipe stage with each instruction being decoded in the instruction decode pipeline.

38. (Previously Presented) The pipelined instruction decoder of claim 37 further comprising:

a pipeline controller coupled to the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline, the pipeline controller to separately control the clocking of each pipe stage of the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline.

39. (Previously Presented) The pipelined instruction decoder of claim 38 wherein

the pipeline controller includes clear logic for each pipe stage, the clear logic to control the invalidation of instructions in each pipe stage of the instruction decode pipeline by setting a valid bit in a respective pipe stage of the valid bit pipeline to indicate an invalid instruction.

40. (Previously Presented) The pipelined instruction decoder of claim 38 wherein

the pipeline controller includes

powerdown logic to analyze the valid indicator of each pipe stage to determine if a next pipe stage is to be powerdowned and to determine if a pipe stage is to be stalled; and

clock control logic to determine if respective clock signals to a pipe stage of the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline are to be stopped to conserve power or preserve data during a stall.

41. (Currently Amended) The pipelined instruction decoder of claim [[38]] 40 wherein

the powerdown logic of the pipeline controller to analyze the valid bit of each pipestage to determine if any pipestage should be stalled,

the powerdown logic including

an exclusive-OR (XOR) gate to exclusively OR a thread identification of a next to last pipe stage with a thread identification of a stall to determined if they match, and

a first AND gate to AND a valid bit of the next to last pipe stage with an output of the XOR gate,

in order to determine if a pipe stage prior to the next to last pipe stage should be stalled.

42. (Previously Presented) The pipelined instruction decoder of claim 41 wherein

the powerdown logic further including,

a second AND gate to AND the valid indicator of the pipe stage for which the determination is being made with the valid indicator of the next pipe stage, and

a third AND gate to AND an output of the second AND gate with an output from the first AND gate,

in order to determine if a pipe stage other than the next to last pipe stage should be stalled.

43. (New) The pipelined instruction decoder of claim 38, wherein

the pipeline controller to squeeze out bubbles of invalid instructions in the instruction decode pipeline by continuously clocking a pipestage with an invalid instruction until a valid instruction is received and overwrites the invalid instruction.

44. (New) The pipelined instruction decoder of claim 38, wherein

the pipeline controller to conserve power by stopping the clocking of the pipelined instruction decoder if there is no valid instruction within the pipelined instruction decoder.

45. (New) The pipelined instruction decoder of claim 38, wherein

the pipeline controller to conserve power by stopping the clocking of circuitry in a pipestage if the thread indentification associated with the pipestage indicates a cleared thread of instructions.

46. (New) The pipelined instruction decoder of claim 38, wherein

the pipeline controller includes

powerdown logic to conserve power.

47. (New) The pipelined instruction decoder of claim 38, wherein

the pipeline controller to invalidate an entire thread of instructions in the instruction decode pipeline associated with a thread identification in response to a clear signal.

48. (New) The pipelined instruction decoder of claim 39, wherein

the clear logic for each pipe stage of the pipeline controller is responsive to a clear signal to invalidate an entire thread of instructions in the instruction decode pipeline associated with a thread identification.

49. (New) An apparatus comprising:

an instruction decode pipeline to decode instructions associated with a plurality of instruction threads, the instruction decode pipeline having a predetermined number of pipe stages;

a valid bit pipeline in parallel with the instruction decode pipeline, the valid bit pipeline having the same predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline, the valid bit pipeline to associate a valid indicator at each pipe stage with each instruction being decoded in the instruction decode pipeline; and

a thread identification pipeline in parallel with the instruction decode pipeline and the valid bit pipeline, the thread identification pipeline having the same predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline and the valid bit pipeline, the thread identification pipeline to associate a thread identification at

each pipe stage with each instruction being decoded in the instruction decode pipeline; and

a pipeline controller coupled to the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline, the pipeline controller to squeeze out bubbles of invalid instructions in the instruction decode pipeline by continuously clocking a pipestage with an invalid instruction until a valid instruction is received and overwrites the invalid instruction.

50. (New) The apparatus of claim 49, wherein

the pipeline controller to conserve power by stopping the clocking of each of the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline if there is no valid instruction within the instruction decode pipeline.

51. (New) The apparatus of claim 49, wherein

the pipeline controller to conserve power by stopping the clocking of circuitry in a pipestage if the thread indentification associated with the pipestage indicates a cleared thread of instructions.

52. (New) The apparatus of claim 49, wherein

the pipeline controller to invalidate an entire thread of instructions in the instruction decode pipeline associated with a thread identification in response to a clear signal.

53. (New) A system comprising:

a memory; and

a microprocessor coupled to the memory, the microprocessor having an instruction decoder, the instruction decoder including

an instruction decode pipeline to decode instructions associated with a plurality of instruction threads, the instruction decode pipeline having a predetermined number of pipe stages;

a valid bit pipeline in parallel with the instruction decode pipeline, the valid bit pipeline having the same predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline, the valid bit pipeline to associate a valid indicator at each pipe stage with each instruction being decoded in the instruction decode pipeline; and

a thread identification pipeline in parallel with the instruction decode pipeline and the valid bit pipeline, the thread identification pipeline having the same

predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline and the valid bit pipeline, the thread identification pipeline to associate a thread identification at each pipe stage with each instruction being decoded in the instruction decode pipeline.

54. (New) The system of claim 53, wherein the instruction decoder further includes a pipeline controller coupled to the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline, the pipeline controller to control the clocking of each pipe stage of the instruction decode pipeline, the valid bit pipeline, and the thread identification pipeline.

55. (New) The system of claim 54, wherein the pipeline controller to squeeze out bubbles of invalid instructions in the instruction decode pipeline by continuously clocking a pipestage with an invalid instruction until a valid instruction is received and overwrites the invalid instruction.

56. (New) The system of claim 54, wherein

the pipeline controller to conserve power by stopping the clocking to each pipestage of the instruction decoder if there is no valid instruction therein.

57. (New) The system of claim 54, wherein

the pipeline controller to conserve power by stopping the clocking of circuitry in a pipestage if the thread indentification associated with the pipestage indicates a cleared thread of instructions.

58. (New) The system of claim 54, wherein

the pipeline controller to invalidate an entire thread of instructions in the instruction decode pipeline associated with a thread identification in response to a clear signal.